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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,393	06/20/2003	Chi-Chun Chen	2002-0066 / 24061.461	8529

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,393	CHEN ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-19* is/are allowed.

6)☒ Claim(s) *20-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/22/03; 12/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/600,393. Currently, claims 1-33 are pending.

Information Disclosure Statement

2. The Gonzalez et al. patent (US 6,294,421) cited in the information disclosure statement filed on 12 February 2004 has been withdrawn. Therefore, the patent has not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. *Claims 20, 25, 27, 30, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonzalez et al. (US 6,383,861 B1).*

The Gonzalez et al. patent (Gonzalez) discloses a method of forming multiple gate insulator layers on a semiconductor substrate (figs. 1-9 and accompanying text). The method comprises the steps of: forming a first dielectric layer 26 over a silicon containing substrate 12 (fig. 3 and col. 4, lines 28-40); selectively removing the first dielectric layer from a second portion 20 of the substrate resulting in a first dielectric gate insulator layer, having a first insulator thickness, located on a first portion 22 of the silicon containing

substrate (fig. 5 and col. 5, lines 11-14); and performing an oxidation procedure to form a second dielectric gate insulator layer, having a second insulator thickness, having a second insulator thickness greater than the first thickness, on the second portion of the silicon containing substrate (fig. 9 and col. 6, lines 7-35), wherein the removal rate of the second dielectric gate insulator layer is higher than the removal rate of the first dielectric layer using a prescribed etchant.[1]

The silicon nitride layer is formed via rapid thermal chemical vapor deposition (RPCVD), and has a thickness between 5 and 30 angstroms, *as recited in claim 25* (col. 4, lines 27-40). The silicon nitride layer 26 is removed from the second portion of the substrate using a hot phosphoric acid solution, *as recited in claim 27* (col. 5, lines 10-24).[2]

The second insulator/dielectric layer 32 is a silicon oxide layer with a thickness between 30 and 80 angstroms, *as recited in claim 30* (col. 6, lines 27-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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[1] The removal rate for silicon oxide is higher than the removal rate of silicon nitride when using HF as an etchant.

[2] *Regarding the claimed language "hot phosphoric acid solution" recited in claims 16 and 30.* The specification does not explicitly define the term "hot." Thus, given the broadest possible reasonable interpretation that is consistent with the specification, the phrase "hot phosphoric acid solution" is interpreted as referring to a heated phosphoric acid solution.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. *Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Wolf et al. (Lu et al. (US 6,693,047 B1).*

Whereas Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator layer 26, to remove an oxide film (col. 3, line 66 - col. 4, line 6), Gonzalez does not teach that either that the first pre-clean procedure is performed in a buffered hydrofluoric (BHF) acid solution comprised of HF in ammonium fluoride, or that the first pre-clean procedure is performed in a dilute HF acid solution comprised of HF in de-ionized water.

The Lu et al. Patent (Lu) discloses a method for recycling semiconductor wafers (col. 2, lines 12-18; col. 3, lines 13-40; and col. 5, lines 26-41). The method comprises removing an oxide film using either a BHF acid solution comprised of HF in ammonium fluoride, or a dilute HF acid solution comprised of HF in de-ionized water (col. 5, lines 26-41).

Since both Gonzalez and Lu are from the same field of endeavor, the purpose for which Lu is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As previously stated, Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator layer 26, to remove an

oxide film. According to Gonzalez, the oxide film can be removed by a variety of ways, which are known in the art (col. 4, lines 4-6). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Lu, by performing the first pre-clean procedure using either a BHF acid solution comprised of HF in ammonium fluoride or a dilute HF acid solution comprised of HF in de-ionized water, since surface treating a semiconductor substrate with HF vapors is known - in the art - to remove an oxide film on the surface of the substrate.

5. *Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Ban et al. (US 5,336,356).*

Whereas Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator/dielectric layer 26, to remove an oxide film (col. 3, line 66 - col. 4, line 6), Gonzalez does not teach that the first pre-clean procedure is a dry procedure performed via use of HF vapors, *as recited in claim 22.* The Ban et al. patent (Ban) discloses a surface treatment apparatus, which cleans or etches an oxide film on the surface of a semiconductor wafer (col. 1, lines 7-13 and col. 2, lines 25-34). In the surface treatment, an oxide film on the surface of a semiconductor substrate is cleaned or etched using HF vapors (col. 2, lines 41-53). Ban discloses several embodiments - for example, see the embodiment described in col. 4, line 46 - col. 6, line 10.

Since both Gonzalez and Ban are from the same field of endeavor, the purpose for which Ban is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As previously stated, Gonzalez discloses performing a first pre-clean procedure, prior to the formation of the first insulator/dielectric layer 26, to remove an oxide film. According to Gonzalez, the oxide film can be removed by a variety of ways, which are known in the art (col. 4, lines 4-6). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Ban, by performing the first pre-clean procedure using HF vapors, since surface treating a semiconductor substrate with HF vapors to remove an oxide film formed thereon is known in the art.

6. *Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Mosleshi et al. (US 4,715,937).*

Whereas Gonzalez discloses that the first insulator/dielectric layer 26 is a silicon nitride layer with a thickness between 5 and 30 angstroms, Gonzalez does not teach forming the silicon nitride using a direct plasma nitridization procedure, *as recited in claim 23*, or using a direct thermal nitridization, as *recited in claim 24*. The Moslehi et al. patent (Moslehi) teaches that direct plasma nitridization and direct thermal nitridization are two known methods used to form thermal nitride (col. 1, lines 21-31).

Since both Gonzalez and Moslehi are from the same field of endeavor, the purpose for which Moslehi is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

As a result of the continuing increase in integration density of integrated circuits, and the reduction in device and circuit geometries, ultra-thin, high quality insulators are needed for gate insulators of IGFETs, storage capacitor insulators of DRAMs, and tunnel dielectrics in nonvolatile memories (Moslehi – col. 1, lines 15-21). Thermal nitrides formed using such techniques as direct plasma nitridization and direct thermal nitridization are of the best alternatives to thermally grown silicon dioxide for these particular applications (Moslehi – col. 1, lines 21-25). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Moslehi by forming the silicon nitride layer 26, a gate insulator layer, using a method selected from one of direct plasma nitridization and direct thermal nitridization, as taught by Moslehi, since thermal nitrides formed using such techniques are of the best alternatives to thermally grown silicon dioxide for applications such as gate insulators.

7. *Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Kim et al. (US 6,391,803 B1)*

Gonzalez does not teach that the silicon nitride layer 26 is formed using atomic layer chemical vapor deposition (ALCVD) procedures, *as recited in claim*

26. The Kim et al. patent (Kim) teaches forming silicon nitride using atomic layer chemical vapor deposition (col. 3, lines).

Since both Gonzalez and Kim are from the same field of endeavor, the purpose for which Kim is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Kim by forming the silicon nitride layer 26 using atomic layer deposition, as taught by Kim, since atomic layer deposition is an alternative to conventional chemical vapor deposition methods (col. 1, lines 13-46). Furthermore, the silicon nitride layer formed using the atomic layer deposition method taught by Kim has an HF wet etching selectivity with respect to silicon oxide (col. 3, lines 5-11).

8. *Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

As discussed above with respect to claim 27, Gonzalez discloses removing the silicon nitride layer 26 from the second portion of the substrate using a hot phosphoric acid solution. Whereas Gonzalez discloses using a hot phosphoric acid solution to remove the silicon nitride layer, Gonzalez does not teach removing the silicon nitride via dry etch procedures using CF_4 or Cl_2 as an etchant. The Wolf et al. reference (Wolf) teaches removing silicon nitride via

dry etch procedures, wherein CF_4 is used as an etchant (page 556 - 2nd par. lines 4-9).

Since both Gonzalez and Wolf are from the same field of endeavor, the purpose for which Wolf is relied upon would have been recognized in the pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Wolf, by removing the silicon nitride layer 26 via dry etch procedures using CF_4 as an etchant, since dry etching using CF_4 etches silicon nitride 2-3 times faster than silicon oxide (page 556 - 2nd par. lines 7-9). Thus, when removing the silicon nitride layer on the second portion 20 of the substrate, the silicon oxide layer 24, which protects the underlying substrate, is substantially unetched.

9. *Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez.*

Whereas Gonzalez discloses performing the second pre-clean procedure (i.e. the pre-clean procedure performed after the removal of the silicon nitride layer 26 from the second portion 20 of the substrate) using a HF acid solution (col. 5, lines 43-53), Gonzalez does not teach that the HF acid solution is a BHF acid solution comprised of HF in ammonium fluoride, as recited in claims 13 and 29, or a dilute HF acid solution comprised of HF in de-ionized water, *as recited in claim 29.* However, since both BHF acid solution and dilute HF acid

solution are HF acid solutions, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to perform the second pre-clean procedure using one or the other.

10. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Ban et al. (US 5,336,356).

Whereas Gonzalez discloses performing a second pre-clean procedure (i.e. performing a second pre-clean after removing the first insulator/dielectric layer 26 from the second portion 20 of the substrate) remove an oxide film (col. 5, lines 43-53), Gonzalez does not teach that the second pre-clean procedure is a dry procedure performed via use of HF vapors, *as recited in claim 31.* The Ban et al. patent (Ban) discloses a surface treatment apparatus, which cleans or etches an oxide film on the surface of a semiconductor wafer (col. 1, lines 7-13 and col. 2, lines 25-34). In the surface treatment, an oxide film on the surface of a semiconductor substrate is cleaned or etched using HF vapors (col. 2, lines 41-53). Ban discloses several embodiments - for example, see the embodiment described in col. 4, line 46 - col. 6, line 10.

Since both Gonzalez and Ban are from the same field of endeavor, the purpose for which Ban is relied upon would have been recognized in the to pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Ban, by performing the

second pre-clean procedure using HF vapors, since surface treating a semiconductor substrate with HF vapors to remove an oxide film formed thereon is known in the art.

11. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez.

Gonzalez does not teach that the oxidation procedure used to form the second dielectric gate insulator is performed at a temperature between 500 to 1100°C. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to perform the oxidation at a temperature between 500 to 1100°C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (*In re Aller,* 105 USPQ 233).

12. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Dobuzinsky et al. (US 5,330.935).

Whereas Gonzalez discloses forming the second gate insulator/dielectric layer 32 using thermal oxidation (col. 6, lines 7-35), Gonzalez does not teach forming the silicon oxide layer 32 via a plasma oxidation procedure in an oxygen-content ambient, *as recited in claim 33.* The Dobuzinsky et al. patent (Dobuzinsky) teaches forming a silicon oxide film using a low temperature plasma oxidation process (col. 6, lines 31-50).

Since both Gonzalez and Dobuzinsky are from the same field of endeavor, the purpose for which Dobuzinsky is relied upon would have been recognized in the to pertinent reference of Gonzalez by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Gonzalez in view of Dobuzinsky, by forming the silicon oxide layer 32 using a plasma oxidation procedure, as taught by Dobuzinsky, since plasma oxidation – as compared to thermal oxidation - is a low temperature oxidation process (Dobuzinsky - col. 3, lines 24-27).

Allowable Subject Matter

13. Claims 1-19 are allowable. The prior art of record does not anticipate, teach or suggest removing the first insulator from the I/O region of the substrate, resulting in a first gate insulator having a first thickness located on the core region of the substrate; and selectively forming a second gate insulator having a second thickness on the I/O region of the substrate.

Response to Arguments

14. Applicant's arguments filed 29 December 2004 have been fully considered but they are not persuasive.

With respect to claim 20, Applicant argues that the thickness of the first insulator in Gonzalez is greater than the thickness of the second insulator. Gonzalez clearly discloses that the thickness of the first insulator is less than the second insulator (see Gonzalez - col. 6, lines 52-55).

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT

21 March 2005

Mary Wilczewski
Primary Examiner